Hanxiang(Dennis) Hao

225 North Ave NW, Atlanta, GA 30332
(404) 889-2325 | hhao40@gatech.edu
https://github.com/DennisHao1211 • https://www.linkedin.com/in/hanxiang-dennis-hao-0a161837b/

EDUCATION

Georgia Institute of Technology (GT), Atlanta, GA — August 2025 – May 2027
Bachelor of Science in Electrical Engineering; GPA: 4.0

Objective Statement

Aspiring ASIC Design Verification Engineer seeking internship or full-time roles in CPU/GPU and SoC verification. Hands-on experience with UVM-based verification, RISC-V pipeline testing across multiple tapeouts, and coverage-driven RTL debugging, with additional exposure to performance-oriented systems (MPI, CUDA).

Skills

Technical

- Design Verification, UVM Testbench Architecture, SystemVerilog Assertions, Formal Verification, Functional Coverage, RTL Design/Debugging, FSM/Timing Verification, Pipeline Testing, DUT Functional Validation, Digital Logic Design, Floorplanning/Macro Placement, Static Timing & DRC Analysis

Tools

- Cadence Xcelium/Genus/VerisiumDebug/Innovus, Synopsys Verdi/VCS, Verilator, Git, Georgia Tech PACE Supercomputing Cluster, Slurm Workload Manager, Yosys, SymbiYosys

Programming

- C/C++, Python, Java, Verilog/SystemVerilog, Makefile/Shell Scripting, MATLAB, RISC-V assembly, CUDA Programing, Parallel Optimization(MPI) Programing, OpenMP

EXPERIENCE

Gatech EIC Lab; Machine Learning System Research Intern — January 2026 - Present

- Implemented training-free sparse attention with dynamic KV cache eviction for Fast-dLLM-v2 (1.5B & 7B),applied Sparse-dLLM to reduce peak memory usage and improve inference throughput of Fast-dLLM-v2 model

Future Computing with Rogues Gallery; Reconfigurable XChaCha FPGA subteam — January 2026 - Present

- Verified the XChaCha cryptographic core using formal verification, proving the correctness of the control logic and interface behavior with OSS CAD Suite

SiliconJackets; Design Verification Engineer — August 2025 - Present

- Verified RISC-V CPU pipeline using UVM and RISC-V random instruction generator; developed assembly tests (matrix multiplication, convolution) to maximize coverage and validate RTL functionality for Tapeout 1, 2, 3

Supercomputing @ GT; High Performance Computing (HPC) Student Researcher — August 2025 - Present

- Developed and optimized MPI- and CUDA-based parallel programs on Georgia Tech's PACE cluster, conducted performance benchmarking and scalability analysis on large-scale matrix computation workloads

PROJECTS

64-bit SystemVerilog Calculator — RTL Design & Verification Project

- Designed a 64-bit unsigned calculator using FSM-based RTL architecture to combine two 32-bit sums
- Implemented control logic, memory-mapped I/O, and timing synchronization for accurate computation
- Built a SystemVerilog testbench to verify RTL functionality through directed and edge-case testing
- Added assertions and performed waveform debugging with Cadence Xcelium and Verisium Debug
- Conducted functional coverage analysis in Verdi, achieving 99% DUT coverage

LICENSES & CERTIFICATION

SystemVerilog Accelerated Verification with UVM Training — *Cadence Design Systems* — November 2025

- Completed 32-hour professional training on UVM 1.2-based verification using Xcelium 2103, covering UVC creation, sequences, TLM, scoreboards, and register modeling